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PATENT NUMBER

ISSUE CLASSIFICATION	Class	Subclass

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED 8/2 Q.A. LR	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/808339	D	~~706~~ 703	14	~~2122~~ 2128	PHAN, THAI

APPLICANTS: Yo Ng Zhou; Antony Fan

TITLE: System and method for simulation of an integrated circuit design using a hierarchical input netlist and divisions along hierarchical boundaries thereof

PTO-2040 12/99

ISSUING CLASSIFICATION

ORIGINAL CLASS	SUBCLASS	CROSS REFERENCE(S) CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)

INTERNATIONAL CLASSIFICATION

☐ Continued on Issue Slip Inside File Jacket

☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.				NOTICE OF ALLOWANCE MAILED	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____				ISSUE FEE	
				Amount Due	Date Paid
☐ The terminal ____months of this patent have been disclaimed.				ISSUE BATCH NUMBER	

(Assistant Examiner) (Date)

(Primary Examiner) (Date)

(Legal Instruments Examiner) (Date)

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